SCHEME AND DETAILED SYLLABUS

FOR

M.TECH TWO YEAR DEGREE COURSE

IN

VLSI DESIGN & EMBEDDED SYSTEMS

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

National Institute of Technology Raipur

Chhattisgarh – 492010

June 2024

SCHEME OF STUDY

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
SEMESTER: I

S.No.	BoS	Sub. Code	Subject Name	Periods/ week			Examination Scheme					Total Marks	Credits L+(T+P)/2
				L	T	P	TA	FE	SE	ESE	Pract. ESE		
1	ECE	EC41111VL	Nanoscale Semiconductor Devices	4	-	-	20	15	15	100	-	150	4
2	ECE	EC41112VL	CMOS Analog IC Design	4	-	-	20	15	15	100	-	150	4
3	ECE	EC41113VL	Advance Digital VLSI Design	4	-	-	20	15	15	100	-	150	4
4	ECE	EC41114VL	Hardware Design with Verilog	4	-	-	20	15	15	100	-	150	4
5	ECE	EC4113XVL	Elective-1	4	-	-	20	15	15	100	-	150	4
6	ECE	EC41121VL	VLSI Design Lab-I	-	-	3	75	-	-	-	50	125	2
7	ECE	EC41122VL	Hardware Design with Verilog lab	-	-	3	75	-	-	-	50	125	2
			Total	20	0	6	250	75	75	500	100	1000	24

TA = Teacher's Assessment, FE = First Exam, SE = Second Exam, ESE = End Semester Exam

Elective- 1

S. No.	Board of Studies	Sub Code	Subject Name
1	ECE	EC41131VL	Nano electronics
2	ECE	EC41132VL	Introduction to CAD Tools
3	ECE	EC41133VL	Embedded Systems & RTOS
4	ECE	EC41134VL	Optoelectronics and Photovoltaics

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
SEMESTER: II

S.No.	BoS	Sub. Code	Subject Name	Periods/ week			Examination Scheme					Total Marks	Credits L+(T+P)/2
				L	T	P	TA	FE	SE	ESE	Pract. ESE		
1	ECE	EC41211VL	Device Fabrication	4	-	-	20	15	15	100	-	150	4
2	ECE	EC41212VL	VLSI System Design	4	-	-	20	15	15	100	-	150	4
3	ECE	EC4123XVL	Elective-2	4	-	-	20	15	15	100	-	150	4
4	ECE	EC4124XVL	Elective-3	4	-	-	20	15	15	100	-	150	4
5	ECE	EC4125XVL	Elective-4	4	-	-	20	15	15	100	-	150	4
6	ECE	EC41221VL	VLSI Design Lab-II	-	-	3	75	-	-	-	50	125	2
7	ECE	EC41222VL	Device Simulation and Fabrication Lab	-	-	3	75	-	-	-	50	125	2
			Total	20	0	6	250	75	75	500	100	1000	24

TA = Teacher's Assessment, FE = First Exam, SE = Second Exam, ESE = End Semester Exam

ELECTIVE-2

S.No.	Board of Studies	Sub Code	Subject Name
1	ECE	EC41231VL	Physical Design Automation
2	ECE	EC41232VL	VLSI Signal Processing
3	ECE	EC41233VL	Mixed Signal Circuit Design
4	ECE	EC41234VL	Signal Processing Algorithms of DSP Architecture

ELECTIVE-3

S.No.	Board of Studies	Sub Code	Subject Name
1	ECE	EC41241VL	Deep Learning Algorithms for VLSI CAD
2	ECE	EC41242VL	MOS Device Modeling and Characterization
3	ECE	EC41243VL	Power Device Modeling
4	ECE	EC41244VL	Thin Film Technology

ELECTIVE-4

S.No.	Board of Studies	Sub Code	Subject Name
1	ECE	EC41251VL	Low Power VLSI Design
2	ECE	EC41252VL	IC Packaging
3	ECE	EC41253VL	Micro-Electro-Mechanical System (MEMS)
4	ECE	EC41254VL	CMOS RF IC Design

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
SEMESTER: III

S.No.	BoS	Sub. Code	Subject Name	Periods/week			Examination Scheme					Total Marks	Credits L+(T+P)/2
				L	T	P	TA	FE	SE	ESE	Pract. ESE		
1	ECE	EC41321VL	Preliminary work on Dissertation	-	-	24	100	-	-	-	200	300	12
2	ECE	EC41322VL	Comprehensive viva-voce and seminar	-	-	-	-	-	-	-	200	200	4
			Total	0	0	24	100	0	0	0	400	500	16

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
SEMESTER: IV

S.No.	BoS	Sub. Code	Subject Name	Periods/week			Examination Scheme					Total Marks	Credits L+(T+P)/2
				L	T	P	TA	FE	SE	ESE	Pract. ESE		
1	ECE	EC41421VL	Dissertation	-	-	32	200	-	-	-	300	500	16
			Total	-	-	32	200	-	-	-	300	500	16

Semester-I

Nanoscale Semiconductor Devices

Theory Periods: 42
Credits: 04 **Code:** EC41111VL

Course Description: This advanced course explores the intricacies of nanoscale semiconductor device. Students will delve into the mathematical formulations, physical principles, and simulation techniques that underlie the accurate representation of semiconductor devices. The course covers a range of nano scale devices, including diodes, transistors, bulk and SOI technology and advanced semiconductor structures. Emphasis is placed on developing in-depth knowledge of the underlying physics and applying that knowledge to construct nanoscale devices for different applications.
Course Content:

MODULE-I
Review of Semiconductor Device Physics: Doping, carrier transport mechanisms, drift, diffusion, thermionic emission, and tunneling; excess carriers, carrier lifetime, recombination mechanisms, metal-semiconductor junction fabrication, Schottky barriers, rectifying ad ohmic contacts, I-V characteristics, hetro-junctions.

MODULE-II
MOS Capacitors and MOSFETs: The MOS capacitor, fabrication, surface charge, accumulation, depletion, inversion, threshold voltage, C-V characteristics, low and high frequency; MOSFET – fabrication, operation, gradual channel approximation, simple charge control model (SCCM), IV characteristics, second-order effects, Velocity saturation, short-channel effects, charge sharing model, hot-carrier effects, gate tunneling; subthreshold operation, drain induced barrier lowering (DIBL) effect, Sub threshold characteristics, short channel effects and the performance of scaled down devices.

MODULE-III
SOI and high K Technology: SOI wafer technology, the electrical properties of advanced SOI materials, Partially and fully depleted SOI MOSFETs, working and operation, merits and demerits, short-channel SOI semiconductor transistors, high-k MOS devices, strained technology, metal gate electrode.
MESFET and HEMTs: fabrication, basic operation, I-V characteristics, high-frequency response, backgating effect, advantage and limitations, HEMTs fabrication, modulation (delta) doping, analysis of III-V heterojunctions, charge control, I-V characteristics, advantage and limitations.

MODULE-IV
FinFET Device Technology: Introduction to FinFET, FinFET Manufacturing Technology, Bulk-FinFET Fabrication, SOI FinFET Process Flow, Long Channel FinFETs, Basic Features of FinFET Devices, FinFET Device Operation, Drain Current Formulation, Small Geometry FinFETs: Physical Effects on Device Performance, Short-channel Effects on Threshold Voltage, Quantum Mechanical Effects, Surface Mobility, High Field Effects.

TEXT BOOKS:

1. Physics of Semiconductor Devices: S. M. Sze, Wiley Eastern, (1981).
2. Semiconductor physics and Devices, Donald Neamen, McGraw-Hill, 3rd edition.
3. Modern Semiconductor Devices for Integrated Circuits, Chenming Hu, Prentice Hall, 2010.

REFERENCE BOOKS:

4. CMOS Circuit Design, Layout and simulation: J. Baker, D.E. Boyce., IEEE press.
5. FinFET Devices for VLSI Circuits and Systems, Samar K. Saha, Taylor and Francis Group, 2020.

Online Resources (NPTEL/MOOC course):

1. https://archive.nptel.ac.in/courses/108/108/108108122/
2. https://archive.nptel.ac.in/courses/108/106/108106181/

CMOS Analog IC Design

Theory Periods: 42
Credits: 04 **Code:** EC41112VL

Course Description: This course is structured with a specific focus on analog IC design. Students will gain a comprehensive understanding of analog CMOS circuit and layout designing techniques. The course includes hands-on TCAD simulations, and projects to reinforce theoretical concepts and provide practical experience in designing complex systems.

Course Content:

MODULE I
MOS IV Characteristics, MOS 2nd order effects, Basic Analog Building Blocks, Switches, and Active Resistors.

MODULE II
Amplifiers: Basic Amplifiers, Current and Voltage sources, Current and voltage references, Voltage regulators.

MODULE III
Current Mirrors, Differential Amplifier, Cascode Amplifiers, High Gain Amplifier Structure, Amplifier design.

MODULE IV
CMOS Operational Amplifiers: Operational Amplifier characteristics, Basic Op-Amp circuits, Frequency response and compensation, Noise sources in Op-Amps, Op-Amp design including Biasing circuits, High performance Op-Amps.

TEXT BOOKS:

1. "Design of Analog CMOS Integrated Circuits", by Behzad Razavi, McGraw Hill.
2. "CMOS Analog Circuit Design" Phillip E. Allen and Douglas R. Holberg. C

REFERENCE BOOKS:

1. "Analog MOS Integrated Circuits for Signal Processing", Roubic Gregorian and Gabor C. Temes, John Wiley & Sons, 1986.
2. "VLSI Design Techniques for Analog and Digital Circuits", Randall Geiger, Phillip E. Allen and Noel Stradder, McGraw Hill International Edition, McGraw Hill.

Online Resources (NPTEL/MOOC course):

1. https://archive.nptel.ac.in/courses/117/106/117106030/

Advanced Digital VLSI Design

Theory Periods: 42
Credits: 04 **Code:** EC41113VL

Course Description: This course is structured with a specific focus on digital IC design. Students will gain a comprehensive understanding of combinational and sequential CMOS circuit and layout designing techniques. The course includes hands-on TCAD simulations, and projects to reinforce theoretical concepts and provide practical experience in designing complex electronic systems.
Course Content:

MODULE I
Basics of CMOS, CMOS and Pseudo-NMOS inverter, VTC, RC interconnect modelling, Driving large capacitive load, noise margin, RC delay minimization, power dissipation, buffer; transistor sizing effect.

MODULE II
Combinational circuit design: static CMOS logic, dynamic CMOS logic, Pseudo-NMOS logic design, transmission gate logic design, NORA Logic, Layout design layers and connectivity, process design rules, layout floorplaning procedure, DRC, LVS, layout design for specialized blocks.

MODULE III
Logical Effort: Logical Effort of Different Digital Circuit Design, Input capacitance, Logical and Electrical effort, parasitic delay, Single stage and Multistage with and without branch network. Design of minimum delay and optimization of best stages.
Layout and stick diagram: Layout Design Rules: Lambda and micron based design rules- stick diagram, Layer properties of various conducting layers in MOS and CMOS technology (diffusion, poly-silicon and metal), Layout design of different CMOS circuit, area estimation.

MODULE IV
Sequential circuit design; Static Latches, Dynamic Latches and Registers, TSPCR, pulse and sense amplifier based registers, Optimization of sequential circuits, CMOS Schmitt trigger, astable and monostable sequential circuits, timing analysis of sequential circuits.

TEXT BOOKS:

1. J. M. Rabaey, A. Chandrakasan, and B. Nikolic, “Digital Integrated Circuits: A design perspective”, 2nd Edition, Pearson Education, ISBN: 978-93-325-7392-5, 2016.
2. Neil H. E. Weste, D. Harris, and A Banerjee, “CMOS VLSI Design: A Circuit and Systems Perspective”, Third edition, Pearson, ISBN: 978-81-775-8568-1, 2005.

REFERENCE BOOKS:

1. Sung-Mo Kang, Y. Leblebici, and C. Kim, “CMOS Digital Integrated Circuits: Analysis and Design”, 4TH edition, McGraw-Hill, ISBN: 978-93-5260-214-8, 2016.
2. J. P. Uyemura, Introduction to VLSI Circuits and Systems, Wiley, ISBN: 978-81-265-0915-7, 2006.
3. Dan Clein, CMOS IC Layout: Concepts, Methodologies, and Tools, Newnes, ISBN: 978-0750671941, 2000.

Online Resources (NPTEL/MOOC course):

1. https://nptel.ac.in/courses/108107129
2. https://nptel.ac.in/courses/108106158

Hardware Design with Verilog

Theory Periods: 42
Credits: 04 **Code:** EC41114VL

Course Description: This course is centered on Electronics System Design with a specific focus on Verilog, and FPGA (Field-Programmable Gate Array) technologies. Students will gain a comprehensive understanding of hardware description languages, digital system design principles, and the implementation of electronic systems on FPGAs. The course includes hands-on lab work, simulations, and projects to reinforce theoretical concepts and provide practical experience in designing complex electronic systems.

Course Content:

MODULE I

Basic concepts of hardware description languages. Hierarchy, Concurrency, Logic, and Delay modeling, Structural, Data-flow and Behavioral styles of hardware description. Variable and signal types, arrays, and attributes. Operators, expressions and signal assignments. Component instantiation.

MODULE II

Use of Procedures and functions, Examples of design using Verilog. Syntax and Semantics of Verilog. Modules, nets and registers, Concurrent and sequential constructs. Tasks and functions, Examples of digital design using Verilog.

MODULE III

Combinational Design using Verilog: Code Conversion, Parity Checker, Comparator Multiplexer, Decoder Decimal Decoder, Full-Adder, Ripple Carry Adder, Carry Look ahead adder, Sign adder, Add/Sub, BCD Adder, Multiplier.

Sequential Design using Verilog: Implementation of Flipflop, counters and registers, Sequential Design with Finite State Machine, RTL design.

MODULE IV

FPGA Architecture and Capabilities, implementing basic digital systems on FPGAs using Verilog. Designing and Implementation of Finite State Machines for FPGA, Synthesis Techniques and Timing Analysis, Placement and Routing; Embedded Hardware and Software Design with FPGA.

TEXT BOOKS:

1. Palnitkar, Samir. Verilog HDL: a guide to digital design and synthesis. Vol. 1. Prentice Hall Professional, 2003.
2. Brown, Stephen, and Zvonko Vranesic. "Digital Logic with VHDL Design." McGRAW HILL company (2005).
3. Vahid, Frank, and Tony D. Givargis. Embedded system design: a unified hardware/software introduction. John Wiley & Sons, 2001.

REFERENCE BOOKS:

1. Cem Unsalan, Bora Tar. Digital System Design with FPGA: Implementation using Verilog and VHDL. McGrawHill, First Edition.
2. Simon Monk. Programming FPGAs Getting Started with Verilog. McGrawHill, First Edition.

Online Resources (NPTEL/MOOC course):

1. https://onlinecourses.nptel.ac.in/noc20_cs63/preview
2. https://onlinecourses.nptel.ac.in/noc24_cs61/preview

Elective 1: Nano electronics

Theory Periods: 42
Credits: 04 **Code:** EC41131VL

Course Description: The course is designed to disseminate knowledge on non-classical CMOS devices and its applications. The course also includes some advanced technology in nanoscale device fabrication and materials.
Course Content:

MODULE I:
Introduction of Nano electronics: Difference between nano science and nano technology, Surface to volume ratio, Approaches to fabrication of nano devices, Scaling of nano electronics devices and their impacts.

MODULE II:
Overview of Nano electronics classical devices and its applications: Vertical MOSFETs, Nano sheet Transistor etc., Bio-sensor, PH sensor, Gas sensor, and Temperature sensor etc.

MODULE III:
Fundamental of advance non classical Nano electronics devices: Fundamental of quantum dot, well, wire and its applications, Resonant Tunneling Transistors, Single electron transistors, new storage such as Memristors, and spintronic.

MODULE IV:
Carbon nanotubes and graphene: Introduction, structure and properties of carbon nanotubes and graphene, Synthesis methods for CNT: CVD, arc discharge, and Laser Evaporation etc.

TEXT BOOKS:

1. Fundamentals of nano electronics by George W Hanson Pearson publications, India 2008.
2. Nanotechnology and Nano Electronics – Materials, devices and measurement Techniques by WR Fahrner – Springer
3. Nanomaterials: Synthesis, properties and applications\edited by A S Edelstein and R C Cammarata (Institute of Physics, UK Series in Micro and Nanoscience and Technology).

REFERENCE BOOKS:

1. Silicon Nanoelectronics by Shunri Odo and David Feny, CRC Press, Taylor & Franicd.
2. Introduction to Nanotechnology, C.P. Poole Jr., F.J. Owens,Wiley (2003), C.P. Poole Jr.,F.J. Owens,Wiley, 2003.
3. Nanoelectronics and Information Technology (Advanced Electronic Materials and Novel Devices), Waser Ranier, Wiley-VCH, 2003.

Online Resources (NPTEL/MOOC course):

1. https://nptel.ac.in/courses/117108047

Elective 1: Introduction to CAD tools

Theory Periods: 42
Credits: 04 **Code:** EC41132VL

Course Description: This course is centered on modelling of semiconductor devices and circuits with a specific focus on SPICE simulation. Students will gain a comprehensive understanding of modelling and the implementation of electronic systems using simulation and provide practical experience in designing complex electronic systems.
Course Content:

MODULE I:
Introduction, CAD and SPICE overview, circuit element and network description.

MODULE II:
Understanding simulation, numerical integration, convergence, time step control, AC, DC and transient analysis

MODULE III:
Diode model, ideal diode, BJT model, MOSFET model, unified charge control model (UCCM), SPICE level 1, 2 and 3berkley short channel IGFET model (BSIM).

MODULE IV:
HBT SPICE model, MESFET SPICE model, high frequency model.

TEXT BOOKS:

1. G. Massobrio and P. Antognetti, Semiconductor Device Modeling with SPICE, 2nd Edition, TMH, 2010
2. Andrei Vladimirescu, The SPICE book, John Wiley & Sons. ISBN-13:978-0471609261, 1994.

REFERENCE BOOKS:

1. Ron M. Kielkowski, Inside SPICE: Overcoming the Obstacles of Circuit xSimulation, McGraw-Hill, ISBN-13 : 978-0079115256, 1994.
2. Paul W. Tuinenga, SPICE: A Guide to Circuit Simulation and Analysis Using PSPice, 3rd Edition, Pearson Education (US), ISBN-13:978-0134420492, 1995.

Online Resources (NPTEL/MOOC course):

1. https://nptel.ac.in/courses/117105147

Elective 1: Embedded system and RTOS

Theory Periods: 42
Credits: 04 **Code:** EC41133VL

Course Description: This course is consists of software and hardware related to embedded systems. The interprocess communication, scheduling of tasks, interconnects between systems are covered in this course. This course would deliver overall knowledge of embedded system and its real time processing activities to the students.
Course Content:

MODULE I:
Hardware Software Co-design and program Modelling: Characteristics of an Embedded System, Quality Attributes of Embedded Systems, Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modelling Language (UML), Hardware Software Tradeoffs.

MODULE II:
REAL-TIME OPERATING SYSTEMS (RTOS) BASED EMBEDDED SYSTEM DESIGN: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling Putting them Altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS.

MODULE III:
PROGRAM MODELING CONCEPTS: Program Models, DFG Models, state Machine Programming Models for Event controlled Program Flow, Modeling of Multiprocessor Systems, UML Modeling.

MODULE IV:
DESIGN EXAMPLES AND CASE STUDIES OF PROGRAM MODELING AND PROGRAMMING WITH RTOS: Case study of Communication between Orchestra Robots, Embedded Systems in Automobile, Case study of an Embedded System for an Adaptive Cruise Control (ACC) System in a Car, Case study of an Embedded System for a Smart Card, Case study of a Mobile Phone Software for Key Inputs.

TEXT BOOKS:

1. Introduction to Embedded System, Shibu K V, McGraw Hill Higher Edition.
2. Embedded Systems Architecture, Programming and Design, Raj Kamal, Second Edition, McGraw Hill.
3. Embedded System Design, Peter Marwedel, Springer.

REFERENCE BOOKS:

1. Embedded System Design – A Unified Hardware/Software Introduction, Frank Vahid, Tony D. Givargis, John Wiley, 2002.
2. Embedded/ Real Time Systems, KVKK Prasad, Dream tech Press, 2005.
3. An Embedded Software Primer, David E. Simon, Pearson Ed. 2005MODULE-I

Online Resources (NPTEL/MOOC course):

1. https://nptel.ac.in/courses/106105159
2. https://nptel.ac.in/courses/108102045

Elective 1: Optoelectronics and Photovoltaics

Theory Periods: 42
Credits: 04 **Code:** EC41134VL

Course Description: This course is structured with a specific focus on optoelectronic phenomenon and its uses to design photovoltaic and other devices. Students will gain a comprehensive understanding of solar cell, and photodetector technologies. The course includes simulation design examples of optoelectronic devices in TCAD to reinforce theoretical concepts and provide practical experience in the subject.
Course Content:

MODULE I:
Optical processes in semiconductors – electron hole recombination, absorption, Franz-Keldysh effect, Stark effect, quantum confined Stark effect, deep level transitions, Auger recombination, Semiconductor p-n junction physics, Schottky barrier diode, heterostructure junctions.

MODULE II:
Si solar Cell Structures: PERC, TopCON, IBC; Charge Collection Probability, QE, Spectral Response, J-V Curve, Resistive Effects, Temperature and Light Intensity effects, Detailed Balance, Tandem Cells; Perovskite solar cell: charge transport layers, perovskite absorber materials, type of perovskite solar cell, design examples in SCAPS 1D.

MODULE III:
Optical Losses in solar cell, Anti-Reflection Coatings, Light Trapping techniques, Current and Voltage Losses due to Recombination, Surface Recombination, Top Contact Design, Emitter Resistance, Contact Resistance, Finger Resistance, Optimization of Finger Spacing, Metal Grid Pattern, design examples in ATLAS.

MODULE IV:
Optical detection – PIN, APD, Modulated barrier photodiode, Schottky barrier photodiode, wavelength selective detection, microcavity photodiodes.

TEXT BOOKS:

1. Jasprit Singh, Semiconductor optoelectronics physics and Technology, McGraw Hill,2019
2. Jenny Nelson, The Physics of Solar cells, Imperial College press, 2003

REFERENCE BOOKS:

1. Semiconductor Optoelectronic Devices, Pallab Bhattacharya, 2nd Ed; Pearson Education, 2002.
2. Photonics: Optical Electronics in modern communication, Amnon Yariv & Pochi, 6th Ed; Oxford Univ. Press, 2006
3. D. Muchahary, S. Bhattarai, A. K. Mahato, S. Maity, "A Brief on Emerging Materials and Its Photovoltaic Application." *Emerging Materials: Design, Characterization and Applications*. Singapore: Springer Nature Singapore, 2022, 421-406. https://link.springer.com/chapter/10.1007/978-981-19-1312-9_10

Online Resources (NPTEL/MOOC course):

1. https://nptel.ac.in/courses/113104084
2. https://nptel.ac.in/courses/115107116
3. PV Education online resource. Link: https://www.pveducation.org/

VLSI Design Lab-I

Theory Periods: 0 **Practical:** 36
Credits: 02 **Code:** EC41121VL

Objectives: To simulate basics of CMOS analog IC and understand the Frequency response, stability, and noise issues in amplifiers. To understand the implementation and testing of linear and nonlinear analog block using simulation.

Course Content:

1. I-V characterization of N-MOSFET and P-MOSFET for long and short channel models.
2. VTC and Transient Analysis of CMOS Inverter for different W/L Ratio of NMOS and PMOS.
3. Simulation and Analysis of NMOS based Inverter circuits such as Diode Connected Load, Depletion Load and PMOS Load.
4. Connect a 2 I/P NAND Gate to an identical NAND Gate such that fan out is 1,2,5,10,50,100. Plot the propagation Delay.
5. Connect a set of 5 inverters in a closed loop in the form of a clock. Estimate the clock frequency.
6. To design layout of CMOS inverter and followed by simulation.
7. Design layout of 2 input NAND/NOR and followed by simulation.
8. To find 3 dB frequency & gain for different values of load & W/L ratio for common source stage with resistive load using P-MOSFET.
9. Simulation & analysis of diode-connected load common source amplifier. Find edge of triode region & gm1, gm2, gain & 3 dB frequencies.
10. DC analysis of source follower using resistive & current source load.
11. AC analysis of common gate amplifiers and calculates input and output impedance.
12. AC analysis differential amplifier & calculate CMRR.
13. Design 2 stages OPAMP for the given specification.
14. Simulation of basic current mirrors using resistive load and cascode current mirror.

Hardware Design with Verilog lab

Theory Periods: 0 **Practical:** 36
Credits: 02 **Code:** EC41122VL

Course Description: This course is centered on the hands-on practice of combinational and sequential circuits using HDL Verilog. Students would gain knowledge on both digital and analog IC design in front end digital platform.

Course Content:

1. Experiments related to language semantics Time Control: delay operator, event control. Assignment Types: procedural, blocking, non-blocking, continuous. Delay through combinational logic and nets
2. Behavioural Coding (examples and problems)
3. Structural Coding (examples and problems)
4. RT-Level Coding (examples and problems)
5. Mixed-Level Coding (examples and problems)
6. Coding of state machines and sequential logic
7. Coding of test benches
8. Coding style for synthesis
9. Entering design constraints and synthesis using "FPGA Express" - Generating timing reports; CLB/gate usage reports; Identifying suitable FPGA device (Xilinix) for design implementation.
10. A mini-project example and suggestions for mini-project topics.

Semester-II

Device Fabrication

Theory Periods: 42
Credits: 04 **Code:** EC41211V

Course Description: This course provides an introduction to the principles and processes of microfabrication, with a focus on semiconductor materials and devices. Students will learn about the key steps in microfabrication, such as photolithography, etching, deposition, and diffusion. They will also learn about the properties of semiconductor materials and how they are used to fabricate electronic devices.
Course Content:

Module I:

Review of semiconductor device processing technologies, clean room, Substrates, Silicon wafer fabrication, Wafer cleaning process.

Module II:

Oxidation techniques, Growth kinetics, Defects in silicon and silicon dioxide, characterization of oxides films, low k and high k dielectrics, Diffusion, Ficks laws, Sheet resistivity and measurement of dopant profiles, Ion implantation, Implantation damage and annealing, transient enhanced diffusion and rapid thermal processing.

Module III:

Lithographic Process: Wafer Cleaning, Barrier Layer Formation, Photoresist Application, Soft Baking / Prebaking, Mask Alignment, Photoresist Exposure and Development, Hard Baking, Mask Generation, Lithography process tools: optical lithography, X-ray and e-beam lithography. Etching Techniques: Wet Chemical Etching, Dry Etching Plasma Systems, Photoresist Removal, Metrology and Critical Dimension Control, Liftoff Process.

Module IV:
Film Deposition: Coating**,** Evaporation, Sputtering, Chemical Vapor Deposition and Epitaxy.
Processes for MEMS: Bulk Micromachining, Surface Micromachining, High-Aspect-Ratio Micromachining, Silicon Wafer Bonding.

TEXT BOOKS:

1. Plummer, J. D. (2009). Silicon VLSI technology: fundamentals, practice and modeling. Pearson Education India.
2. G. S. May and S. M. Sze, Fundamentals of Semiconductor Fabrication, Wiley India,

REFERENCE BOOKS:

1. Jaeger, R. C. (2002). Introduction to microelectronic fabrication (2nd ed.).
2. Campbell, S. A. (2001). The science and engineering of microelectronic fabrication.
3. River, NJ: Prentice Hall. Peter VanZant, “Microchip Fabrication, Sixth Edition: A Practical Guide to Semiconductor Processing” McGraw Hill Professional, 2014.

Online Resources (NPTEL/MOOC Course):

1. https://archive.nptel.ac.in/courses/113/106/113106062/
2. https://archive.nptel.ac.in/courses/108/101/108101089/

VLSI System Design

Theory Periods: 42
Credits: 04 **Code:** EC41212VL

Course description: This course offers an exploration into the ARM, intel and DSP processor architectures and instruction set, designed to nurture, and develop students' unique knowledge into a system designer. Through a combination of interactive lectures, assignments, and individualized feedback, students will engage in various forms of digital system design software, including Verilog. The course also explores data path and control path design of processor using basic building blocks.

Course Content:

Module I:
Essential features of Instruction set architectures of CISC and RISC and the implications for implementation as VLSI chips; CISC Instruction-set implementation, and RT-Level optimization through hardware flow-charting (without/with pipelining concepts); Micro programming approaches for implementation of control part of the processor; Handling of Instruction boundary interrupts, Immediate interrupts and traps in processors; Pipelined implementation of RISC Instruction Sets; Benefits and problems of pipeline execution; Hazards of various types and pipeline stalling; Scheduling(static and dynamic) and forwarding to reduce/minimize pipeline stalls.

Module II:
Introduction to programmable DSP architectures; architecture and assembly language of TMS320C6X; Synthesis of DSP architectures; Scheduling and source allocation for DSP architectures; Scheduling algorithms, CORDIC and distributed arithmetic architectures.

Module III:
Data path design: addition, subtraction, zero/one detector, comparators: magnitude and equality detector; counters: arbitrary, synchronous, and asynchronous; parity and error correcting codes, shifters: logical, arithmetic and barrel; multiplication: Booth's algorithm, pipeline multiplier array.

Module IV:
Timing issues in Digital Circuits: Timing classification of digital System, Synchronous Design Timing basics, clock skew, clock jitter and their combined impact; Finite state machine: FSM with data path, program state machine model.

TEXT BOOKS:

1. C. Hamacher, Z. Vranesic, and S. Zaky, "Computer organization" fifth edition, McGraw Hill, ISBN: 0-07-120411-3, 2011.
2. J.M. Rabaey, A. Chandrakasan, and B. Nikolic, "Digital Integrated Circuits: A design perspective", 2nd Edition, Pearson Education, ISBN: 978-93-325-7392-5, 2016.

REFERENCE BOOKS:

1. D.D. Gajski, S.A.A. Gerstlauer, G. Schirner, "Embedded system design: Modelling, Synthesis, Verification", Springer, ISBN-178-1-4419-0503-1, 2009.
2. F. Vahid and, T. Givargis, "Embedded system design: A unified hardware/software approach", John Wiley and Sons, ISBN-978-0-471-38678-0, 2001.

Online Resources (NPTEL/MOOC course):

1. https://nptel.ac.in/courses/108106177
2. https://nptel.ac.in/courses/108103179

Elective 2: Physical Design Automation

Theory Periods: 42
Credits: 04 **Code:** EC41231VL

Course Description: This course provides the need and the importance of physical design automation in VLSI cycle. It covers the complete process step wise which includes floor planning, placement and partitioning. Students will be able to know how; various aspects of routing algorithms are used in design cycle. Timing analysis gives the idea to enhance the performance of a design and clocking tree synthesis describes the routing of clock nets. This course will also describe how noise analysis, layout compaction and physical verification is done before the chip is designed.
Course Content:

Module I:
Design Representation, Physical Design, Structural level design flow, Physical level design flow, Configurable logic blocks, Cell Layout, Partitioning, Floor planning, Placement.

Module II:
Routing: Grid Routing, Retracing, Lees algorithm, Global Routing, Hadlock's algorithm, Line search algorithm, Detailed Routing, Basic Left Edge Algorithm, Power and Ground Routing, Dogleg router algorithm.

Module III:
Clock Design, Clock Network Synthesis, Time Closure, Time driven Placement, Physical Synthesis, Performance Driven design flow, Timing Optimization, Design Rule check, Layout compaction.

Module IV:
Testing: Fault Modelling, Fault Simulation, Test Pattern generation, Boundary Scan, Built in self-test.

TEXT BOOKS:

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic.
2. Sadiq M Sait, "VLSI Physical Design Automation: Theory and Practice.

REFERENCE BOOKS:

1. Gerez, Sabih H., "Algorithms for VLSI Design Automation", John Wiley & Sons.
2. Drechsler, Rolf, "Evolutionary Algorithms for VLSI CAD" Springer Science & Business Media.
3. Trimberger, Stephen M., "An Introduction to CAD for VLSI", Springer Science & Business Media.

Online Resources (NPTEL/MOOC course):

1. **https://nptel.ac.in/courses/106105161**
2. **https://nptel.ac.in/courses/108107380**

Elective 2: VLSI Signal Processing

Theory Periods: 42
Credits: 04 **Code:** EC41232VL

Course Description: This course provides introduce students to the fundamentals of VLSI signal processing and expose them to examples of applications. Design and optimize VLSI architectures for basic DSP algorithms.
Course Content:

Module I:
Introduction to VLSI DSP Systems: Need of VLSI DSP algorithms. main DSP Blocks and typical DSP Algorithms. Fixed point /Floating point Representation; Floating point Arithmetic Implementation, Architectures of Adders/Multipliers; CORDIC, representation of DSP algorithms: Block Diagram, signal flow graph, data flow graph, dependence graph.

Module II:
Iteration Bound: Data flow graph representations, loop bound and iteration bound, longest path matrix algorithm, iteration bound of Multi rate data flow graphs.

Module III:
Pipelining and Parallel Processing: Pipelining and parallel processing of FIR digital filters, pipeline interleaving in digital filters: signal and multichannel interleaving.

Module IV:
Retiming, Unfolding and Folding: retiming techniques; algorithm for unfolding, Folding transformation, Techniques of retiming, Unfolding & Folding.
Systolic Array Architecture: Systolic Array Architecture: Methodology of systolic array architecture, FIR based Systolic Array, Selection of Scheduling Vector, Matrix multiplication of systolic array.

TEXT/REFERENCE BOOKS:

1. VLSI Digital Signal Processing System: Design and implementation by K.K. Parhi.
2. Digital Signal Processing with Field Programmable Gate Arrays Uwe Meyer-Baese, Springer.

REFERENCE BOOKS

1. FPGA-based Implementation of Signal Processing Systems. by Roger Woods, John Mcallister, WILEY.

Online Resources (NPTEL/MOOC course):

1. **https://archive.nptel.ac.in/courses/108/105/108105157/**

Elective 2: Mixed Signal Circuit Design

Theory Periods: 42
Credits: 04 **Code:** EC41233VL

Course Description: This course provides a comprehensive exploration of mixed signal circuits, focusing on the integration of both analog and digital components within a single system. Students will delve into the design principles, analysis techniques, and practical considerations involved in mixed signal circuitry. The curriculum covers topics such as switched capaciors, analog-to-digital conversion (ADC), digital-toanalog conversion (DAC), signal processing, noise analysis, and the coexistence of analog and digital elements. Through theoretical study, practical simulations, and hands-on projects, students will gain the skills needed to design and analyze mixed signal circuits for a variety of applications.
Course Content:

Module I:
Overview of mixed signal circuits and their importance, Historical context and evolution of mixed signal design, review of design of current mirrors, differential amplifiers, CMOS operational transconductance amplifiers, design of single ended telescopic cascode, folded cascode and two-stage amplifiers.

Module II:
Basic S/H circuit, effect of charge injection, compensating for charge injection, bias dependency, bias independent S/H. Switched capacitor circuits, design of switched capacitor amplifiers and integrators, effect of opamp finite gain, bandwidth and offset, circuit techniques for reducing effects of opamp, imperfections, switches and charge injection and clock feed-through effects.

Module III:
Design of sample and hold and comparators, Fundamentals of data converters; Nyquist rate A/D converters (Flash, interpolating, folding flash, SAR and pipelined architectures); Nyquist rate D/A converters - voltage, current and charge mode converters, hybrid and segmented converters); Oversampled A/D and D/A converters.

Module IV:
PLLs: Basic Phase-Locked Loop Architecture, Voltage Controlled Oscillator, Divider Phase Detector, Loop Filer, The PLL in Lock, Liberalized Small-Signal Analysis, Second-Order PLL Model , Limitations of the Second-Order Small-Signal Model, PLL Design.

TEXT BOOKS:

1. Marcel Pelgrom. Analog to Digital Conversion. Springer, 2017.
2. Mourad Fakhfakh, Esteban Tlelo Cuautle, Rafael Castro Lopez. Analog/RF and Mixed Signal Circuit Systematic Design. Springer, 2013.
3. Phillip E Allen, Douglas R Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 2011.
4. Jacob Baker, "CMOS Mixed-Signal circuit design", A John Willy & Sons, inc., publications, 2003.

REFERENCE BOOKS:

1. R.Gregorian - Introduction to CMOS opamps and comparators.
2. D.Johns and K.Martin - Analog integrated circuit design
3. B.Razavi - Monolithic Phase-locked loops and clock recovery circuits: Theory and design

Online Resources (NPTEL/MOOC course):

1. https://archive.nptel.ac.in/courses/117/106/117106030/

Elective 2: Signal Processing Algorithms of DSP Architecture

Theory Periods: 42
Credits: 04 **Code**: EC41234VL

Course Description: To provide sound foundation of digital signal processing (DSP) architectures and designing efficient VLSI architectures for DSP systems.
Course Content:

Module I:
Transformations for retiming**:** Folding and unfolding DSP programs. Bit level arithmetic structures- parallel multipliers, interleaved floor plan and bit plan based digital filters. Bit serial multipliers. Bit serial filter design and implementation, Canonic signed digit arithmetic, Distributed arithmetic.

Module II:
Redundant arithmetic**:** redundant number representations carry free radix 2 addition and subtraction, Hybrid radix 4 addition. Radix 2 hybrid redundant multiplication architectures, data format conversion. Redundant to non-redundant converter. Numerical strength reduction.

Module III:
Synchronous pipelining**:** clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs. Wave pipelining, constraint space diagram and degree of wave pipelining. Implementation of wave-pipelined systems. Asynchronous pipelining.

Module IV:
Scaling versus power consumption**:** Power analysis, power reduction techniques, power estimation techniques. Low power IIR filter design. Low power CMOS lattice IIR filter.

TEXT BOOKS:

1. K.K. Parhi: VLSI Digital Signal Processing systems, John Wiley, 1999.
2. Proakis, Digital Signal Processing, PHI, Second edition.

REFERENCE BOOKS

1. Lars Wanhammar, DSP Integrated Circuits, Academic Press, First edition, 1999.
2. K.K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, John Wiley, 2007.

Online Resources (NPTEL/MOOC course):

1. https://nptel.ac.in/courses/108106149

Elective 3: Deep Learning Algorithms for VLSI CAD

Theory Periods: 42
Credits: 04 **Code:** EC41241VL

Course Description: This course provides the introduction of the machine learning and deep learning and their architecture. It gives insights to use various ML/DL techniques for optimization in VLSI process flow.
Course Content:

Module I:
Over view of machine learning (ML) and deep learning (DL), Potential application of ML/DL in VLSI Design and Technology, ML/DL approaches for VLSI CAD.

Module II:
Machine Learning for Compact Lithographic Process Models, Mask Synthesis, Physical Verification, and Physical Design.

Module III:
Gaussian Process based Wafer-Level Correlation Modeling and Its Applications, Machine Learning Approaches for IC Manufacturing Yield Enhancement, Efficient Process Variation Characterization by Virtual Probe, Machine Learning for VLSI Chip Testing and Semiconductor Manufacturing Process Monitoring and Improvement.

Module IV:
Extreme Statistics in Memories, Fast Statistical Analysis Using Machine Learning, Fast Statistical Analysis of Rare Circuit Failure Events, Learning from Limited Detain VLSI CAD.

TEXT BOOKS:

1. Machine Learning in VLSI Computer-Aided Design, Ibrahim (Abe) M. Elfadel, Duane S. Boning, Xin Li, Springer 2019.
2. An Artificial Intelligence Approach to VLSI Routing, R. Joobbani, Springer Science & Business Media, 2012.

REFERENCE BOOKS:

1. Machine Learning Applications in Electronic Design Automation, Ren, Haoxing, Springer Nature, 2023.
2. Optimization in VLSI Design, Lu. Bing, Springer Science & Business Media, 2001.

Elective 3: MOS Device Modeling and Characterization

Theory Periods: 42
Credits: 04 **Code:** EC41242VL

Course Description: Review the operation and modeling of the MOS Capacitor and MOSFETs, Analyze and model small dimension effects in modern MOSFETs, Review the MOSFET fabrication processes and familiarize the use of TCAD tools in semiconductor device and process simulation.
Course Content:

Module I:
2-terminal MOS device: threshold voltage modeling (ideal case as well as considering the effects of Qf, Φms and Dit.).

Module II:
C-V characteristics (ideal case as well as taking into account the effects of Qf, Qm and Dit); MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Qf, Qm and Dit).

Module III:
4-terminal MOSFET: threshold voltage (considering the substrate bias); above threshold I-V modeling (SPICE level 1, 2, 3 and 4).

Module IV:
Subthreshold current model; scaling; effect of threshold tailoring implant (analytical modeling of threshold voltage using box approximation); buried channel MOSFET.Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer's model).

TEXT BOOKS:

1. D.G. Ong, "Modern MOS Technology: Processes, Devices and Design", McGraw Hill, 1984.
2. Y. Taur and T. H. Ning, "Fundamentals of modern VLSI Devices" Cambridge Univ. Press, 1998.

REFERENCE BOOKS

1. S.M. Sze, "Physics of Semiconductor Devices" Wiley,1981.

NPTEL

1. https://archive.nptel.ac.in/courses/117/106/117106033/
2. https://onlinecourses.nptel.ac.in/noc23_ee35/preview

Elective 3: Power Device Modeling

Theory Periods: 42
Credits: 04 **Code:** EC41243VL

Course Description: To study and familiarization of power devices. Power semiconductor devices are also important as low power devices.
Course Content:

Module I:
Review of conventional power devices IGBT, MESFET, HEMT.

Module II:
Physics of power devices; power BJT, IGBT, MESFET, GaAs/GaN devices, power MOSFETs etc., and working principle of power devices.

Module III:
Types of power MOSFETs, lateral, vertical, importing Super junction concept in power devices, High-k, MOS devices and applications.

Module IV:
Design of power MOSFETs using Wide-bandgap semiconductor materials such as GaAs, SIC, GaN etc. Radiation Hardened, Radiation Hardened Power Devices.

TEXT BOOKS:

1. D. A. Grant and J. Grower, Power MOSFETs theory and application. John Wiley and Sons, 1989.
2. B. J. Baliga," Advanced Power MOSFET Concepts". Springer, 2010.

REFERENCE BOOKS:

1. S. K. Gandhi, VLSI Fabrication Principles Silicon and Gallium Arsenide, 2nd ED. Wiley Student Edition, 2003.
2. B. J. Baliga, Silicon Carbide Power Devices. World Scientific Publishing Co. Pte. Ltd., 2005.
3. D. Neamen, Semiconductor Physics and Devices. McGraw-Hill Education (India) Pvt Limited, 2003.

Online Resources (NPTEL/MOOC course):

1. https://nptel.ac.in/courses/108105066

Elective 3: Thin Film Technology

Theory Periods: 42
Credits: 04 **Code**: EC41244VL

Course Description: The course covers the importance of thin film technology and nanofabrication, vacuum technology, various physical and chemical methods of thin film fabrication and various applications of thin films including sensors.

Course Content:

Module I:
Vacuum technology: Clean Room – Clean room technology and its Classes. Principles of vacuum pumps in range of 10 - 2 torr to 10-11 torr, principle of different vacuum pumps: roots pump, rotary, oil diffusion pump, turbo molecular pump, cryogenic-pump, ion pump, Penning and pressure control.

Module II:
Conditions for the formation of thin films: Environment for thin film deposition, deposition parameters and their effects on film growth, formation of thin films (sticking coefficient, formation of thermodynamically stable cluster – theory of nucleation).

Module III:
Physical Vapour Deposition techniques: Thermal evaporation, resistive evaporation, Electron beam evaporation, Laser ablation, Flash and Cathodic arc deposition.

Module IV:
Electrical discharges used in thin film deposition: Sputtering, Glow discharge sputtering, Magnetron sputtering, Ion beam sputtering, R.F sputtering, Triode sputtering, Ion Plating, Difference between thin films and coating.

TEXT BOOKS:

1. Thin Film Phenomenon by K.L. Chopra, McGraw-Hill
1. Vacuum Physics and Techniques by T.A. Delchar, Chapman and Hall Evaporation: Nucleation and Growth Kinetics" by J.P. Hirth and G.M. Pound, Pergamon Press

REFERENCE BOOKS:

2. Methods of Experimental Physics (Vol 14) by G.L. Weissler and R.W. Carlson "Vacuum Physics and Technology"
3. A User's Guide to vacuum Technology by J.F. O'Hanlon, John Wiley and Sons

Online Resources (NPTEL/MOOC course):

1. https://nptel.ac.in/courses/113104075
2. https://archive.nptel.ac.in/noc/courses/noc19/SEM1/noc19-me30/

Elective 4: Low Power VLSI Design

Theory Periods: 42
Credits: 04 **Code:** EC41251VL

Course Description: The objective of this course is to provide students with understanding of sources of power consumption of CMOS circuits**.** This course also discussed about Power Reduction Techniques and Low Power Logic design Styles**.**
Course Content:

Module I:
Introduction of Low Power: Overview of MOS and its applications, Low power design methodology, Impact of scaling on devices and circuits, Different parameters such as delay, noise margin and power dissipation, Working and comparison of different Inverters and its assessment. Design aspect of different Inverters.

Module II:
Estimation of Power in CMOS, Sources of power dissipation in CMOS, Derivation of dynamic power dissipation such as switching power, short circuit, and glitch dissipation. Different parameters to minimize the leakage power in CMOS.

Module III:
Design and Techniques used for Low-Power CMOS Circuits: Overview of Variable threshold CMOS, Multiple Threshold CMOS, Stack Approach, Sleepy Keeper Approach, Clock Gating, Encoding.

Module IV:
Low-Power Memories: Overview of RAM and ROM, RAM Architecture & Sense Amplifier, working of 4T RAM, 6T RAM, 8T etc., 1 DRAM, 3T DRAM, Butter flying curve, Bit cell ratio, pull up ratio, Stable Noise Margin forhold, read and write operation.

TEXT BOOKS:

1. J. B. Kuo and J-H. Lou, Low-Voltage CMOS VLSI Circuits, Wiley, 1999.
2. K. Roy and S. C. Prasad, Low-Power CMOS VLSI Circuit Design, Wiley, 2000.

REFERENCE BOOKS

1. A.P. Chandrakasan and R. W. Broderson, Low-Power CMOS Design, IEEE Press, 1998.
2. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, Digital Integrated Circuits: A Design Perspective, Second Edition, PH/Pearson, 2003.

Online Resources (NPTEL/MOOC course):

1. **https://archive.nptel.ac.in/courses/106/105/106105034/**

Elective 4: IC Packaging

Theory Periods: 42
Credits: 04 **Code:** EC41252VL

Course Description: This course provides a comprehensive exploration of Integrated Circuit (IC) packaging, covering various packaging technologies, materials, and techniques used in semiconductor packaging. Students will delve into the complexities of packaging design, considering factors such as thermal management, interconnection technologies, and the impact on electrical, mechanical, and thermal performance. The curriculum includes an in-depth study of different packaging types, materials, and the trade-offs involved in the design process. Practical projects, case studies, and hands-on experiences will be integral components, preparing students for roles in the semiconductor industry, manufacturing, and product development.

Course Content:

Module I:
Introduction to IC Packaging Technologies: Overview of IC packaging and its significance, Historical context and evolution of packaging technologies. Introduction to packaging types: through-hole, surface-mount, ball grid array.

Module II:
Packaging Materials and Interconnection Techniques: Study of materials used in semiconductor packaging. Interconnection techniques: wire bonding, flip-chip, and solder bump technologies.

Module III:
Thermal Management in IC Packaging: Principles of thermal management in IC packaging. Techniques for heat dissipation and cooling, Case studies: Analyzing thermal management strategies, Signal and Power Integrity Considerations, Signal integrity challenges in IC packaging, Power integrity considerations and solutions.

Module IV:
Reliability in IC Packaging: Factors affecting reliability in IC packaging, Testing and validation techniques for packaged ICs, Advanced Topics in IC Packaging, Emerging trends in IC packaging technologies, Advanced materials and techniques.

TEXT BOOKS:

1. John H. Lau. Semiconductor Advanced Packaging. Springer, 2021.
2. King-NingTu, Chih Chen, Hung-Ming Chen. Electronic Packaging Science and Technology. John Wiley and Sons Inc., 2022.

Reference Book for IC packaging

1. Rao R. Tummala, Fundamentals of Microsystems Packaging, McGraw Hill, NY, 2001.
2. William D. Brown, Advanced Electronic Packaging, IEEE Press, 1999.

Online Resources (NPTEL/MOOC course):

1. https://archive.nptel.ac.in/courses/108/108/108108031/

Elective 4: Micro-Electro-Mechanical System (MEMS)

Theory Periods: 42
Credits: 04 **Code:** EC41253VL

Course Description: The Microelectromechanical devices are new generation devices which are used as the sensor, transducers and actuators. Many of these devices are being developed and they are replacing many bulky electro-mechanical devices. The fabrication technology design and analysis of these devices is the major part of this course.
Course Content:

Module I:
Historical Background: Silicon Pressure sensors, Micromachining, Micro Electro Mechanical Systems Micro-fabrication and Micromachining: Integrated Circuit Processes, Bulk Micromachining.

Module II:
Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA) Physical Microsensors. Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples: Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors Micro actuators.

Module III:
Electromagnetic and Thermal micro actuation, Mechanical design of micro actuators, Micro actuator examples, microvalves, micropumps, micromotors- Micro actuator systems: Success Stories, Ink-Jet printer heads, Micro-mirror TV Projector Surface Micromachining.

Module IV:
One or two sacrificial layer processes, Surface micromachining requirements, Polysilicon surface micromachining, Other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials, Surface Micro machined Systems: Success Stories, Micromotors, Gear trains, Mechanisms.

TEXT BOOKS

1. An introduction to Micro electro mechanical systems Engineering by Nadim Malut and Kirt Williams – Second edition – Artech House, Inc, Boston
2. Micro electro mechanical systems Design by James J Allen- CRC Press – Taylor and Francis Group

REFERENCE BOOKS

1. Springer Hand Book of Nano Technology by Bharath Bhushan – Springer
2. Nano and Micro electro Mechanical systems by Sergey Edward Lysherski – CRC Press.
3. MEMS & Micrsystems Design and Manufacture-Tai-Ran Hsu, Tata McGraw Hill

Online Resources (NPTEL/MOOC course):

1. **https://nptel.ac.in/courses/117105082**

Elective 4: CMOS RF IC Design

Theory Periods: 42
Credits: 04 **Code**: EC41254VL

Course Description: This course explores the principles and techniques of designing RF (Radio Frequency) and HF (High-Frequency) circuits. Topics include passive components used in RF and HF circuits, impedance matching, resonant circuits, filters, and basic RF amplifiers. Students will gain an understanding of the behaviour of components at high frequencies, distributed effects, signal propagation, and RF circuit characteristics. The course may cover impedance transformation, matching networks, RF power amplification, mixers, oscillators, and their applications in wireless communication, radio systems, radar, and other high-frequency electronic devices.
Course Content:

Module I:
Characteristics of passive IC components at RF frequencies: interconnects, resistors, capacitors, inductors and transformers, Transmission lines Classical two-port noise theory, noise models for active and passive components, Noise figure, Friis equation, Nonlinearity and cascaded stages, Sensitivity and dynamic range, Passive impedance transformation, MMIC.

Module II:
RF diodes and transistors: RF diodes, MESFET, HEMT and their circuit models, matching and biasing networks, noise and distortion in RF system, Design of RF system building blocks.

Module III:
High frequency amplifier design: zeros as bandwidth enhancers, shunt-series amplifier, fT doublers, neutralization and unilateralization. Low noise amplifier design: LNA topologies, impedance matching, power constrained noise optimization, linearity and large signal performance, noise canceling LNAs, Constant gm biasing, current reusing technique.

Module IV:
RF Mixers: noise in RF circuits, balanced mixers; low noise mixers, microwave transmitters and receivers.

TEXT BOOKS:

1. Thomas H. Lee, Cambridge, The Design of CMOS Radio-Frequency Integrated Circuits, UK: Cambridge University Press, 2004.
2. Behzad Razavi, RF Microelectronics, Prentice Hall, 1998.

REFERENCE BOOKS

1. R. Jacob Baker, H.W. Li, D.E. Boyce, “CMOS Circuit Design, layout and Simulation”, PHI, 1998.
2. Y.P. Tsividis, “Mixed Analog and Digital Devices and Technology”, TMH, 1996

Online Resources (NPTEL/MOOC course):

1. https://www.digimat.in/nptel/courses/video/117102012/L01.html

VLSI Design lab-II

Theory Periods: 0 **Practical:** 36
Credits: 02 **Codes:** EC41221VL

Objectives: To familiar with CAD and SPICE for device/circuit simulation. To understand various techniques for device/circuit design methodologies.

Course Content:

- Use of CAD and SPICE for device/circuit design.
- Logic design and Layout design
- Design any two 4bit DAC and compare their performance
- Design any two ADC and compare their performance (delay, power, area, power delay products, gain error, settling error etc)
- Design of switched capacitor filters
- Circuit extraction from layout and verification by simulation of extracted circuits.

TEXT/REFERENCE BOOKS:

1. SPICE manual
2. IRSIM manual
3. MAGIC manual
4. Xilinx Corporation, "FPGA technology for Nineties" Xilinx
5. Handbook, 1992.

Device Simulation and Fabrication Lab

Theory Periods: 0 **Practical:** 36
Credits: 02 **Codes:** EC41222VL

Objectives: To simulate basics of semiconductor device and understand the device physics and analysis of the various device dimension effect on device performance. This fabrication lab will help the students to understand the fabrication process flow with hands-on training.

Course Content:

Section-I:

- Design and Simulation of 2D/3D NMOS Channel Length 20nm or higher.
- Design and Simulation of 2D/3D PMOS Channel Length 20nm or higher
- Implementation of SOI/Bulk 2D/3D Nanowire FET & Tunnel FET using TCAD.
- Implementation of SOI/Bulk Dual Gate FET & Dual Gate Junctionless FET.
- Design and Implementation of SOI/Bulk FINFET device upto 5nm technology using GDS2MESH and GENIUS.

Section- II:

- Introduction to fabrication facility and Safety Training
- Standard Cleaning using RCA-1 &2 and Ultra sonication
- Sample preparation using Spin-Coater, Dip-Coater, Sol-Gel method and characterization
- Silicon Oxide/Nitride wet etching using BOE
- Some experiments of diode/ 2 terminal devices using thin film deposition techniques and Electrical characterization.